

### 3A, 36V, 500kHz Synchronous Step-Down Converter

#### General Description

The RT7272A is a high efficiency, current mode synchronous step-down DC-DC converter that can deliver up to 3A output current over a wide input voltage range from 4.5V to 36V. The device integrates a 150mΩ high side and a 80mΩ low side MOSFET to achieve high conversion efficiency up to 95%. The current mode control architecture supports fast transient response and simple compensation circuit.

A cycle-by-cycle current limit function provides protection against shorted output and an internal soft-start eliminates input current surge during start-up. The RT7272A provides complete protection functions such as input under-voltage lockout, output under-voltage protection, over-current protection and thermal shutdown.

The RT7272A is available in the thermal enhanced SOP-8 (Exposed Pad) package.

#### Ordering Information

RT7272A □ □

- Package Type  
SP : SOP-8 (Exposed Pad-Option 2)
- Lead Plating System  
G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

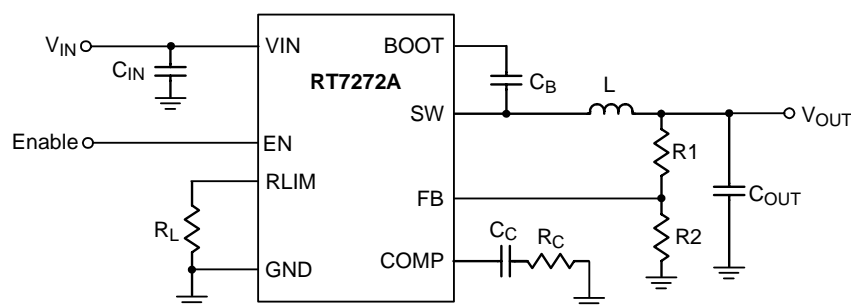
#### Features

- 4.5V to 36V Input Voltage Range
- 3A Output Current
- Internal N-MOSFETs
- Current Mode Control
- Fixed Frequency Operation : 500kHz
- Adjustable Output Voltage from 0.8V to 30V
- High Efficiency Up to 95%
- Stable with Low ESR Ceramic Output Capacitors
- Cycle-by-Cycle Current Limit
- Input Under Voltage Lockout
- Output Under-Voltage Protection
- Thermal Shutdown Protection
- Adjustable Current Limit
- RoHS Compliant and Halogen Free

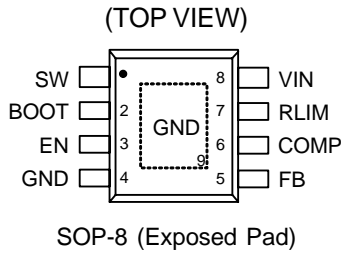
#### Applications

- Distributed Power Systems
- Pre-Regulator for Linear Regulators
- Notebook Computers
- Point of Load Regulator in Distributed Power System
- Digital Set-Top Boxes
- Personal Digital Recorders
- Broadband Communications
- Flat Panel TVs and Monitors
- Vehicle Electronics

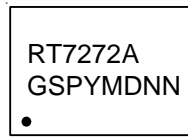
#### Simplified Application Circuit



## Pin Configuration



## Marking Information

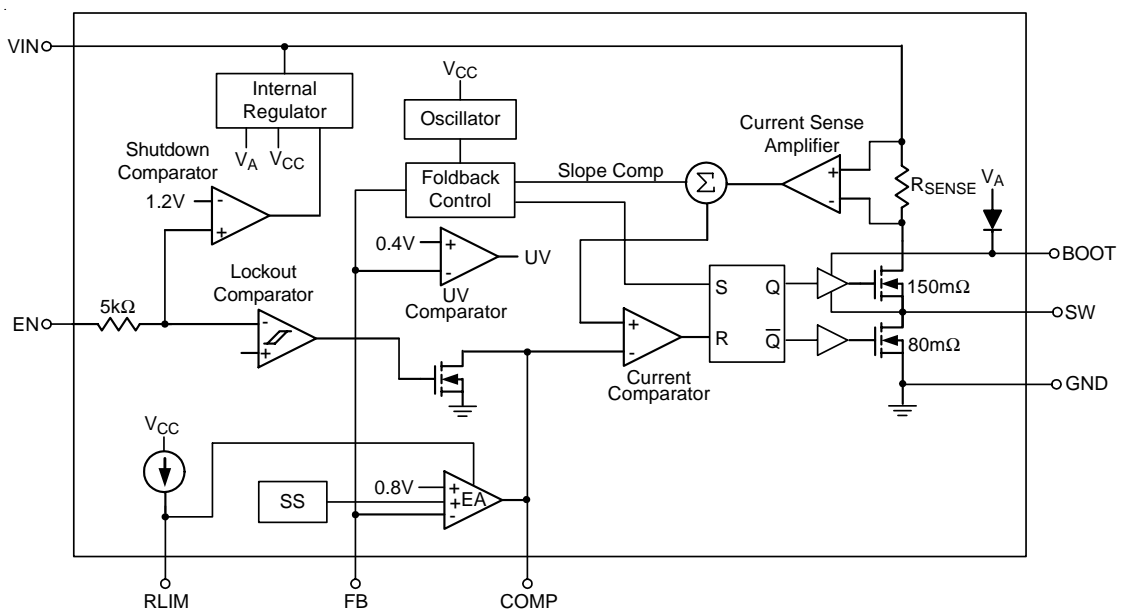


RT7272AGSP : Product Number  
YMDNN : Date Code

## Functional Pin Description

Pin No.	Pin Name	Pin Function
1	SW	Switch node. Connect to external L-C filter.
2	BOOT	Bootstrap supply for high-side gate drive. A 100nF or greater capacitor is recommended to connect from BOOT pin to SW pin.
3	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
4, 9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum thermal dissipation.
5	FB	Feedback input. This pin is connected to the converter output. It is used to set the output of the converter to regulate to the desired value via a resistive divider.
6	COMP	Compensation node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP to GND is required.
7	RLIM	Current limit setting. Connect to a resistor to determine current limit.
8	VIN	Power input. The input voltage range is from 4.5V to 36V. Must bypass with a suitable large ceramic capacitor.

## Functional Block Diagram



## Operation

The RT7272A is a constant frequency, current mode synchronous step-down converter. In normal operation, the high side N-MOSFET is turned on when the S-R latch is set by the oscillator and is turned off when the current comparator resets the S-R latch. While the high side N-MOSFET is turned off, the low side N-MOSFET is turned on to conduct the inductor current until next cycle begins.

### Error Amplifier

The error amplifier adjusts its output voltage by comparing the feedback signal ( $V_{FB}$ ) with the internal 0.8V reference. When the load current increases, it causes a drop in the feedback voltage relative to the reference. The error amplifier's output voltage then rises to allow higher inductor current to match the load current.

### Oscillator

The internal oscillator runs at fixed frequency 500kHz. In short circuit condition, the frequency is reduced to 75kHz for low power consumption.

### Internal Regulator

The regulator provides low voltage power to supply the internal control circuits and the bootstrap power for high side gate driver.

### Soft-Start (SS)

An internal current source charges an internal capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft-start interval. The typical soft-start time is 2ms.

### Current Setting

The current limit of high side MOSFET is adjustable by an external resistor connected to the RLIM pin. The current limit range is from 1.9A to 7A. When the inductor current reaches the current limit threshold, the COMP voltage will be clamped to limit the inductor current.

### UV Comparator

If the feedback voltage ( $V_{FB}$ ) is lower than 0.4V, the UV Comparator will go high to turn off the high side MOSFET. The output under voltage protection is designed to operate in Hiccup mode. When the UV condition is removed, the converter will resume switching.

### Thermal Shutdown

The over temperature protection function will shut down the switching operation when the junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will automatically resume switching.

## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage,  $V_{IN}$  ----- -0.3V to 40V
- Switch Voltage,  $SW$  ----- -0.3V to 40.3V  
 $SW$  ( $t < 10ns$ ) ----- -5V to 46V
- $V_{BOOT} - V_{SW}$  ----- -0.3V to 6V
- Other Pins Voltage ----- -0.3V to 40V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ C$   
SOP-8 (Exposed Pad) ----- 2.041W
- Package Thermal Resistance (Note 2)  
SOP-8 (Exposed Pad),  $\theta_{JA}$  -----  $49^\circ C/W$   
SOP-8 (Exposed Pad),  $\theta_{JC}$  -----  $15^\circ C/W$
- Lead Temperature (Soldering, 10 sec.) -----  $260^\circ C$
- Junction Temperature -----  $150^\circ C$
- Storage Temperature Range -----  $-65^\circ C$  to  $150^\circ C$
- ESD Susceptibility (Note 3)  
HBM (Human Body Model) ----- 2kV

## Recommended Operating Conditions (Note 4)

- Supply Input Voltage,  $V_{IN}$  ----- 4.5V to 36V
- Junction Temperature Range -----  $-40^\circ C$  to  $125^\circ C$
- Ambient Temperature Range -----  $-40^\circ C$  to  $85^\circ C$

## Electrical Characteristics

( $V_{IN} = 12V$ ,  $C_{IN} = 20\mu F$ ,  $T_A = 25^\circ C$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Shutdown Supply Current		$V_{EN} = 0V$	--	0.5	3	$\mu A$
Quiescent Current	$I_Q$	$V_{EN} = 3V$ , $V_{FB} = 0.9V$	--	0.9	1.2	mA
Feedback Reference Voltage	$V_{REF}$	$4.5V \leq V_{IN} \leq 36V$	0.788	0.8	0.812	V
High Side Switch On-Resistance	$R_{DS(ON)1}$		--	150	--	$m\Omega$
Low Side Switch On-Resistance	$R_{DS(ON)2}$		--	80	--	$m\Omega$
High Side Switch Leakage Current		$V_{EN} = 0V$ , $V_{SW} = 0V$	--	0	10	$\mu A$
Upper Switch Current Limit Range	$U_{OC}$		1.9	--	7	A
Upper Switch Current Limit	$U_{OC}$ (Note 5)	Min. duty cycle, $R_{LIM} = 57.6k\Omega$	1.9	2.5	3.1	A
		Min. duty cycle, $R_{LIM} = 84.5k\Omega$	2.7	3.5	4.2	
		Min. duty cycle, $R_{LIM} = 137k\Omega$	4.8	5.5	6.3	
Lower Switch Current Limit		From drain to source	--	1.5	--	A

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Oscillation Frequency	f <sub>OSC1</sub>		450	500	550	kHz
Short Circuit Oscillation Frequency	f <sub>OSC2</sub>	V <sub>FB</sub> = 0V	--	75	--	kHz
Maximum Duty Cycle	D <sub>MAX</sub>	V <sub>FB</sub> = 0.7V	--	90	--	%
Minimum On-Time	t <sub>ON_MIN</sub>		--	100	--	ns
EN Input Voltage	Logic-High	V <sub>IH</sub>	1.4	1.65	2	V
	Logic-Low	V <sub>IL</sub>	1.2	1.45	1.9	
EN Input Voltage Logic-High Hysteresis	ΔV <sub>IH</sub>		--	0.2	--	V
Input Under Voltage Lockout Threshold	V <sub>UVLO</sub>	V <sub>IN</sub> rising	3.9	4.1	4.3	V
Input Under Voltage Lockout Hysteresis	ΔV <sub>UVLO</sub>		--	250	--	mV
Thermal Shutdown	T <sub>SD</sub>		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT <sub>SD</sub>		--	20	--	°C
COMP to Current Sense Transconductance	G <sub>CS</sub>	ΔI <sub>COMP</sub> = ±10μA	--	4.7	--	A/V
Error Amplifier Transconductance	G <sub>EA</sub>		--	1000	--	μA/V
Load Regulation	ΔV <sub>LOAD</sub>		--	--	0.05	%/A
Line Regulation	ΔV <sub>LINE</sub>	V <sub>IN</sub> = 4.5V to 36V	--	--	0.1	%

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

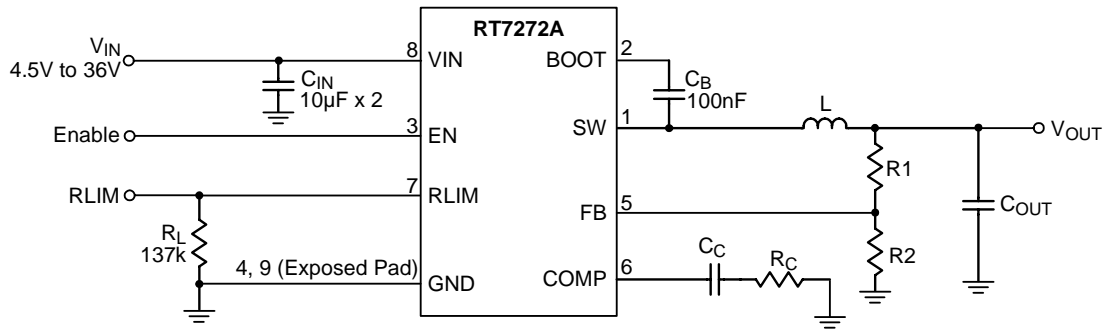
**Note 2.** θ<sub>JA</sub> is measured at T<sub>A</sub> = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ<sub>JC</sub> is measured at the exposed pad of the package.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 4.** The device is not guaranteed to function outside its operating conditions.

**Note 5.** R<sub>LIM</sub> (kΩ) = [U<sub>OC</sub> x 24.14 x (1 + 0.024 x (U<sub>OC</sub> – 3.5)) – 1.3], where U<sub>OC</sub> is desired upper switch peak current limit value.

## Typical Application Circuit

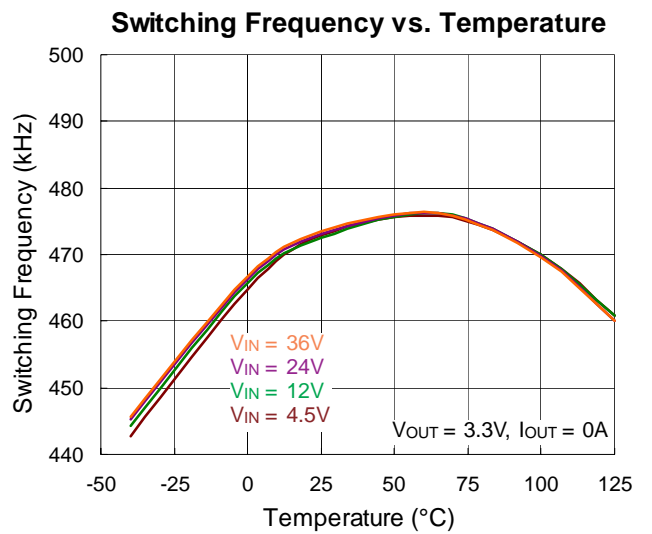
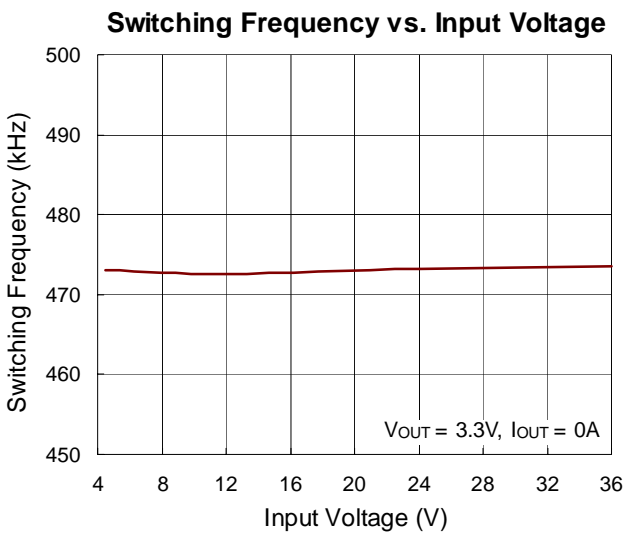
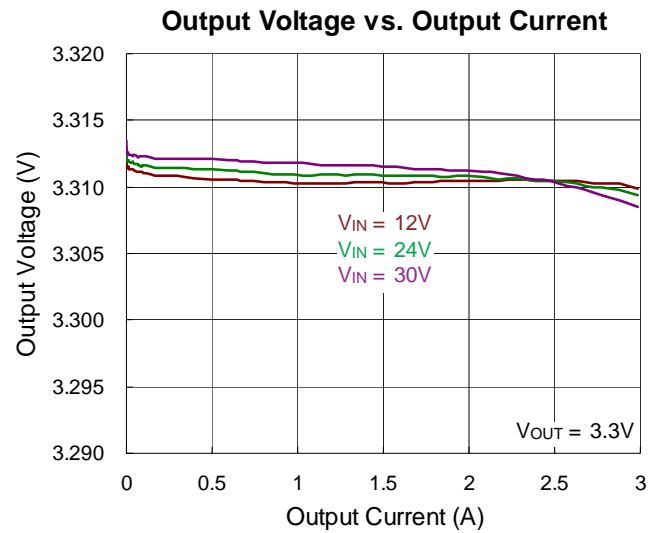
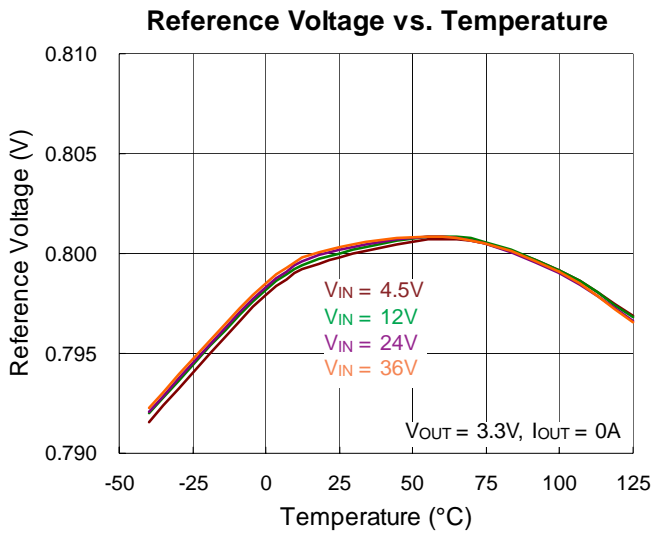
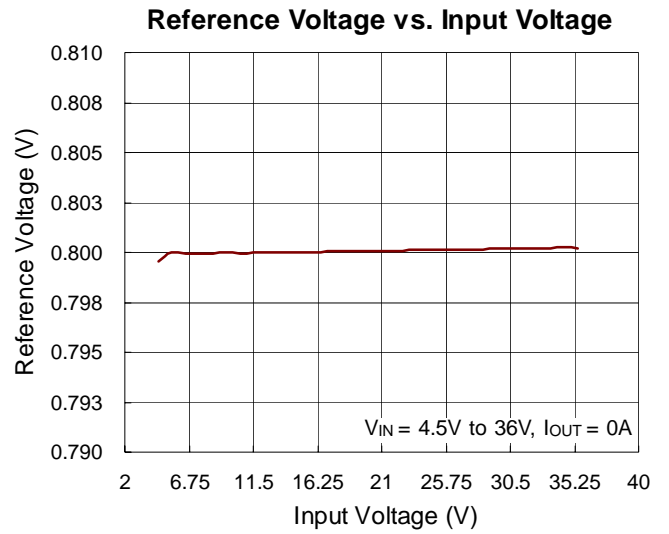
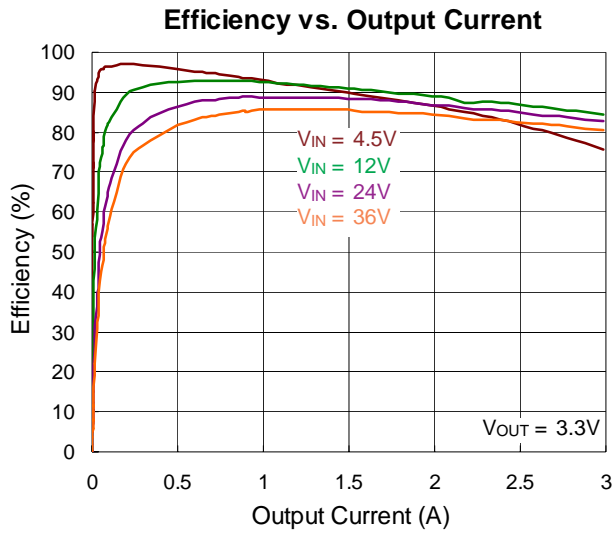


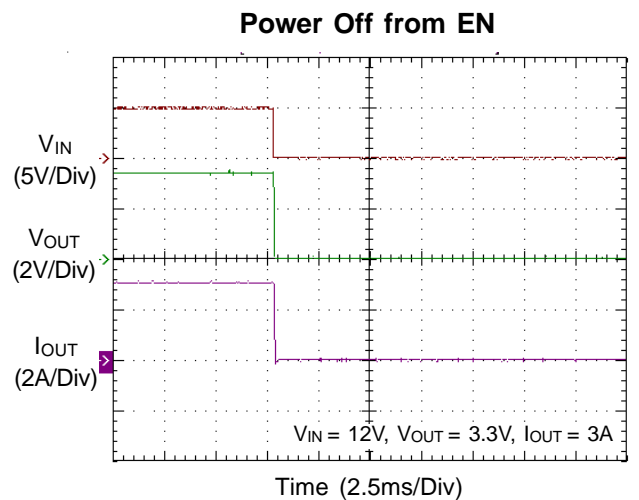
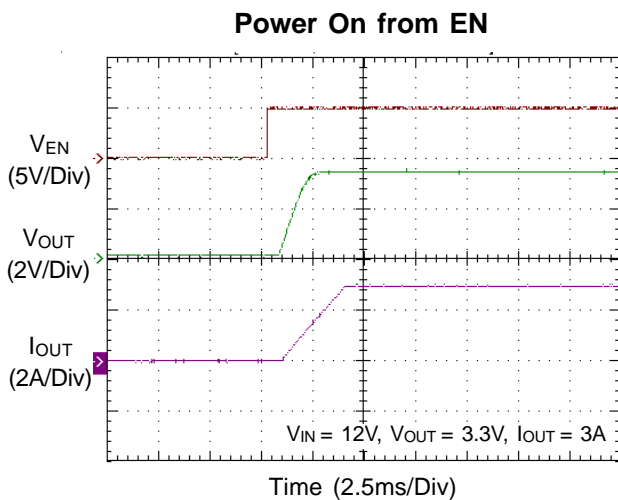
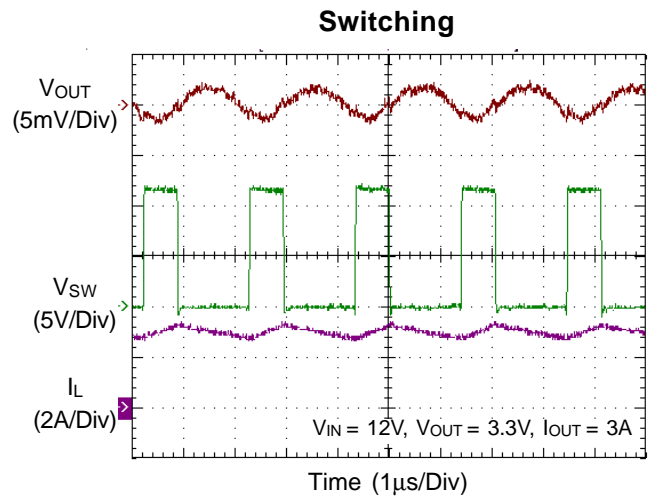
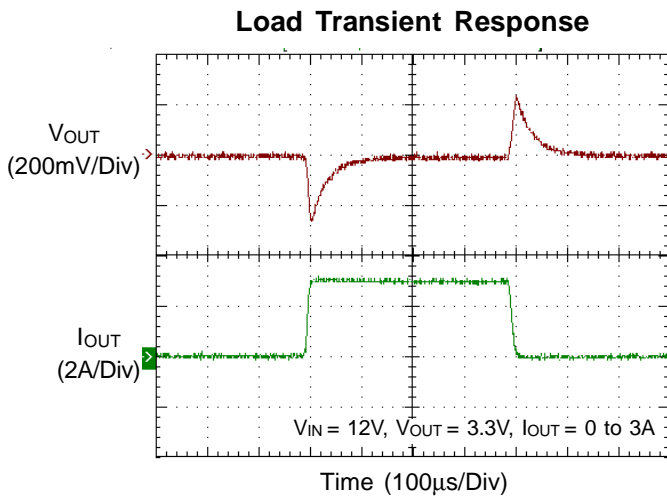
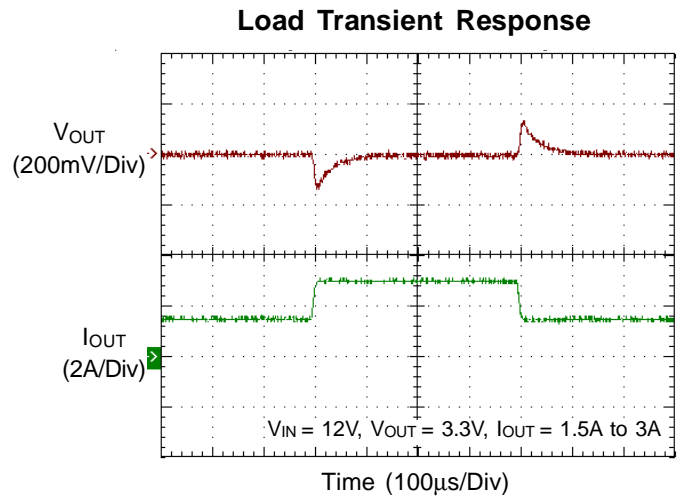
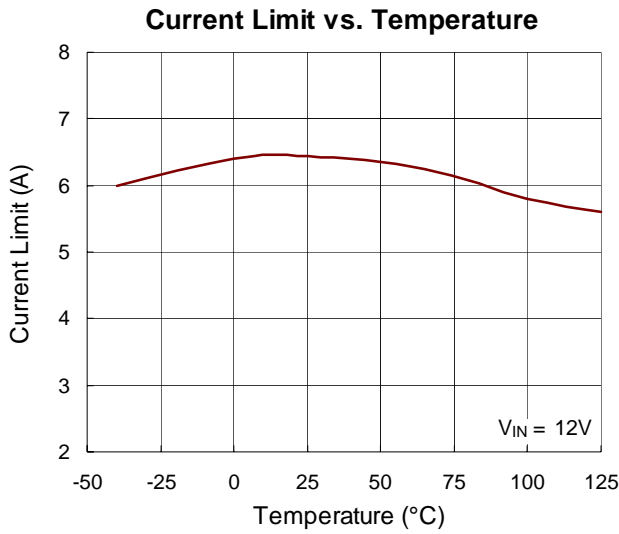
**Table 1. Suggested Component Values**

V <sub>OUT</sub> (V)	R <sub>1</sub> (kΩ)	R <sub>2</sub> (kΩ)	R <sub>C</sub> (kΩ)	L (µH)	C <sub>C</sub> (nF)	C <sub>OUT</sub> (µF)
12	47	3.35	47	10	2.7	22 x 2
8	27	3	36	8.2	2.7	22 x 2
5	62	11.8	24	6.8	2.7	22 x 2
3.3	75	24	16	4.7	2.7	22 x 2
2.5	25.5	12	12	3.6	2.7	22 x 2
1.2	30	60	6.8	2.2	2.7	22 x 2

Note : All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

**Typical Operating Characteristics**







## Application Information

### Output Voltage Setting

The resistive divider allows the FB pin to sense the output voltage as shown in Figure 1.

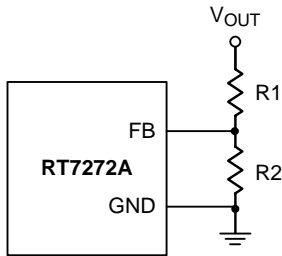


Figure 1. Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF} \left( 1 + \frac{R1}{R2} \right)$$

Where  $V_{REF}$  is the reference voltage (0.8V typ.).

### External Bootstrap Diode

Connect a 0.1μF low ESR ceramic capacitor between the BOOT and SW pins. This capacitor provides the gate driver voltage for the high side MOSFET.

It is recommended to add an external bootstrap diode between an external 5V and BOOT pin for efficiency improvement when input voltage is lower than 5.5V or duty ratio is higher than 65% .The bootstrap diode can be a low cost one such as IN4148 or BAT54. The external 5V can be a 5V fixed input from system or a 5V output of the RT7272A. Note that the external boot voltage must be lower than 5.5V

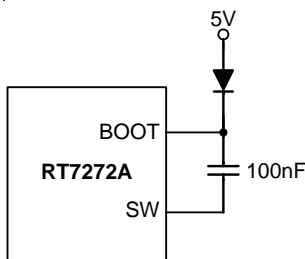


Figure 2. External Bootstrap Diode

### Chip Enable Operation

The EN pin is a device enable input. Pulling the EN pin to logic low that is typically less than the set threshold voltage 1.45V, the device shuts down and enters to low quiescent current state about 3μA. The regulator starts switching again once the EN pin voltage exceeds the threshold voltage 1.65V. For external timing control, the EN pin can also be externally pulled high by adding a  $R_{EN}$  resistor and  $C_{EN}$  capacitor from the VIN pin (see Figure 3).

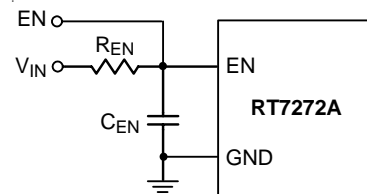


Figure 3. Enable Timing Control

An external MOSFET can be added to implement digital control on the EN pin when no system voltage above 2.5V is available, as shown in Figure 4. In this case, a 100kΩ pull-up resistor,  $R_{EN}$ , is connected between  $V_{IN}$  and the EN pin. MOSFET Q1 will be under logic control to pull down the EN pin.

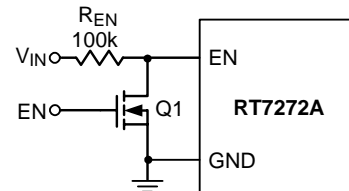


Figure 4. Digital Enable Control Circuit

### Under-Voltage Protection

#### Hiccup Mode

The RT7272A provides Hiccup Mode Under-Voltage Protection (UVP). When the  $V_{FB}$  voltage drops below 0.4V, the UVP function will be triggered to shut down switching operation. If the UVP condition remains for a period, the RT7272A will retry automatically. When the UVP condition is removed, the converter will resume operation. The UVP is disabled during soft-start period.

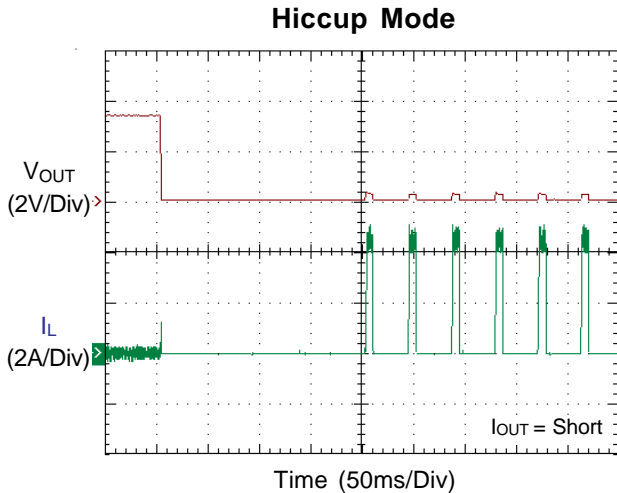


Figure 5. Hiccup Mode Under Voltage Protection

**Over-Temperature Protection**

The RT7272A features an Over-Temperature Protection (OTP) circuitry to prevent from overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds 150°C. Once the junction temperature cools down by approximately 20°C, the converter will resume operation. To maintain continuous operation, the maximum junction temperature should be lower than 125°C.

**Inductor Selection**

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current  $\Delta I_L$  increases with higher  $V_{IN}$  and decreases with higher inductance.

$$\Delta I_L = \left[ \frac{V_{OUT}}{f \times L} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. High frequency with small ripple current can achieve the highest efficiency operation. However, it requires a large inductor to achieve this goal.

For the ripple current selection, the value of  $\Delta I_L = 0.24(I_{MAX})$  will be a reasonable starting point. The largest ripple current occurs at the highest  $V_{IN}$ . To guarantee that the ripple current stays below the specified maximum, the inductor value should be chosen according to the following equation :

$$L = \left[ \frac{V_{OUT}}{f \times 0.24 \times I_{(MAX)}} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

The inductor's current rating (caused a 40°C temperature rising from 25°C ambient) should be greater than the maximum load current and its saturation current should be greater than the short circuit peak current limit. Please see Table 2 for the inductor selection reference.

**Table 2. Suggested Inductors for Typical Application Circuit**

Component Supplier	Series	Dimensions (mm)
TDK	VLF10045	10 x 9.7 x 4.5
TDK	SLF12565	12.5 x 12.5 x 6.5
TAIYO YUDEN	NR8040	8 x 8 x 4

**C<sub>IN</sub> and C<sub>OUT</sub> Selection**

The input capacitance,  $C_{IN}$ , is needed to filter the trapezoidal current at the Source of the high side MOSFET. To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The approximate RMS current equation is given :

$$I_{RMS} = I_{OUT(MAX)} \frac{V_{OUT}}{V_{IN}} \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT} / 2$ . This simple worst case condition is commonly used for design because even significant deviations do not offer much relief.

Choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design.

For the input capacitor, two 10µF low ESR ceramic capacitors are suggested. For the suggested capacitor, please refer to Table 3 for more details.

The selection of  $C_{OUT}$  is determined by the required ESR to minimize voltage ripple.

Moreover, the amount of bulk capacitance is also a key for  $C_{OUT}$  selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response as described in a later section.

The output ripple,  $\Delta V_{OUT}$ , is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8fC_{OUT}} \right]$$

The output ripple will be the highest at the maximum input voltage since  $\Delta I_L$  increases with input voltage. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirement. Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input,  $V_{IN}$ . At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at  $V_{IN}$  large enough to damage the part.

**Thermal Considerations**

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

Where  $T_{J(MAX)}$  is the maximum operation junction temperature ,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating conditions specification of the RT7272A, the maximum junction temperature is 125°C. The junction to ambient thermal resistance  $\theta_{JA}$  is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance  $\theta_{JA}$  is 75°C/W on the standard JEDEC 51-7 four-layers thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (75^\circ\text{C/W}) = 1.333\text{W}$$

(min.copper area PCB layout)

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (49^\circ\text{C/W}) = 2.04\text{W}$$

(70mm<sup>2</sup>copper area PCB layout)

The thermal resistance  $\theta_{JA}$  of SOP-8 (Exposed Pad) is determined by the package architecture design and the PCB layout design. However, the package architecture design had been designed. If possible, it's useful to increase thermal performance by the PCB layout copper design. The thermal resistance  $\theta_{JA}$  can be decreased by adding copper area under the exposed pad of SOP-8 (Exposed Pad) package.

As shown in Figure 6, the amount of copper area to which the SOP-8 (Exposed Pad) is mounted affects thermal performance. When mounted to the standard SOP-8 (Exposed Pad) pad (Figure 6.a),  $\theta_{JA}$  is 75°C/W. Adding copper area of pad under the SOP-8 (Exposed Pad) (Figure 6.b) reduces the  $\theta_{JA}$  to 64°C/W. Even further, increasing the copper area of pad to 70mm<sup>2</sup> (Figure 6.e) reduces the  $\theta_{JA}$  to 49°C/W.

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance  $\theta_{JA}$ . The Figure 7 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power dissipation allowed.

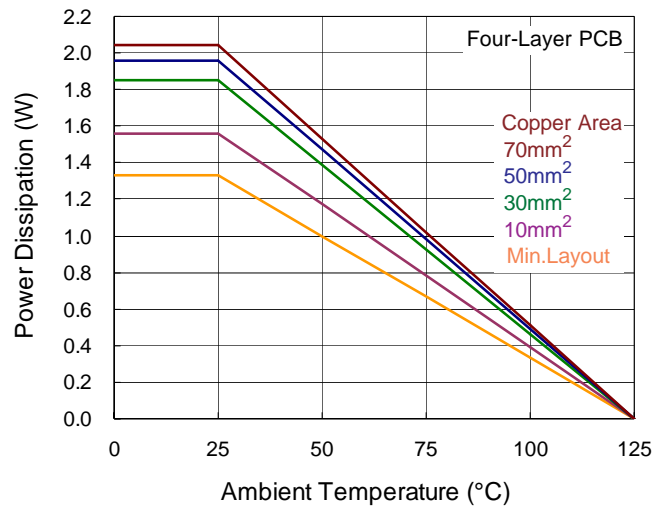
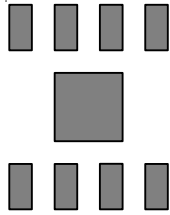
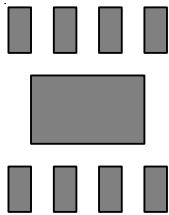


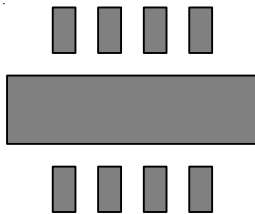
Figure 7. Derating Curve of Maximum Power Dissipation



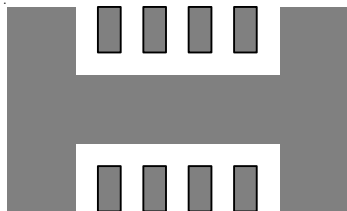
(a) Copper Area =  $(2.3 \times 2.3) \text{ mm}^2$ ,  $\theta_{JA} = 75^\circ\text{C/W}$



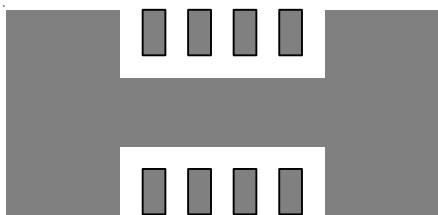
(b) Copper Area =  $10\text{mm}^2$ ,  $\theta_{JA} = 64^\circ\text{C/W}$



(c) Copper Area =  $30\text{mm}^2$ ,  $\theta_{JA} = 54^\circ\text{C/W}$



(d) Copper Area =  $50\text{mm}^2$ ,  $\theta_{JA} = 51^\circ\text{C/W}$



(e) Copper Area =  $70\text{mm}^2$ ,  $\theta_{JA} = 49^\circ\text{C/W}$

Figure 6. Thermal Resistance vs. Copper Area Layout Design

**Layout Considerations**

For best performance of the RT7272A, the following layout guidelines must be strictly followed.

- ▶ Input capacitor must be placed as close to the IC as possible.
- ▶ SW should be connected to inductor by wide and short trace. Keep sensitive components away from this trace.
- ▶ The  $R_L$  resistor, compensator and feedback components must be connected as close to the device as possible.

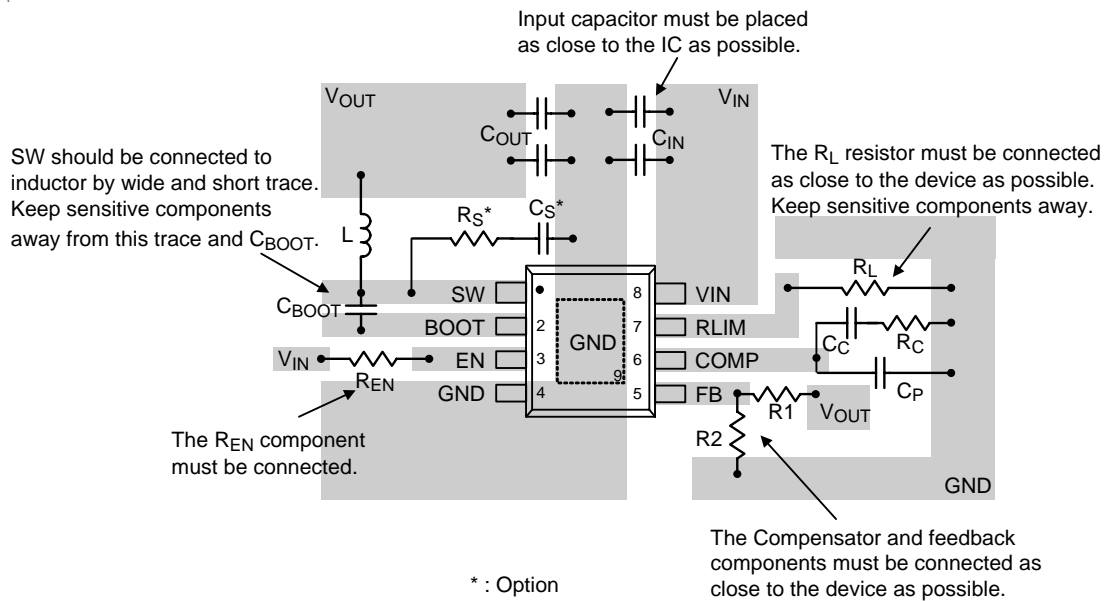
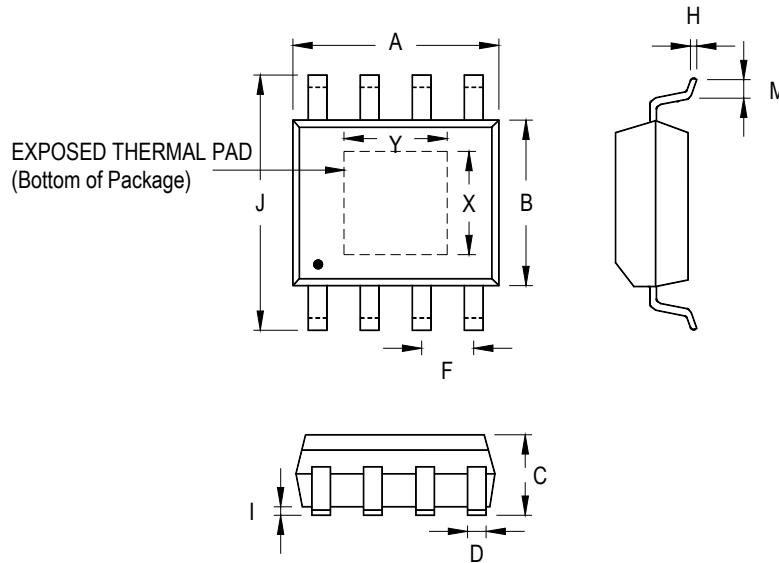


Figure 8. PCB Layout Guide

Table 3. Suggested Capacitors for  $C_{IN}$  and  $C_{OUT}$

Location	Component Supplier	Part No.	Capacitance ( $\mu F$ )	Case Size
$C_{IN}$	MURATA	GRM32ER71H475K	4.7	1206
$C_{IN}$	TAIYO YUDEN	UMK325BJ475MM-T	4.7	1206
$C_{IN}$	MURATA	GRM31CR61E106K	10	1206
$C_{IN}$	TDK	C3225X5R1E106K	10	1206
$C_{IN}$	TAIYO YUDEN	TMK316BJ106ML	10	1206
$C_{OUT}$	MURATA	GRM31CR60J476M	47	1206
$C_{OUT}$	TDK	C3225X5R0J476M	47	1210
$C_{OUT}$	MURATA	GRM32ER71C226M	22	1210
$C_{OUT}$	TDK	C3225X5R1C22M	22	1210

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	4.801	5.004	0.189	0.197	
B	3.810	4.000	0.150	0.157	
C	1.346	1.753	0.053	0.069	
D	0.330	0.510	0.013	0.020	
F	1.194	1.346	0.047	0.053	
H	0.170	0.254	0.007	0.010	
I	0.000	0.152	0.000	0.006	
J	5.791	6.200	0.228	0.244	
M	0.406	1.270	0.016	0.050	
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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